



09/419,439.

COPY

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

February 2, 2005

Patent Number: 6,839,833  
Issued: January 4, 2005  
Title: System and Method for  
Controlling the Entry of  
Instructions into a Pipeline of  
an Instruction Processor

Name of Patentees: Thomas D. Harnett  
John S. Kuslak  
Leroy J. Longworth

Our File: RA 5274 (5268)

Customer No.: 27516

Attn: Certificate of Correction Branch  
Commissioner for Patents  
P O Box 1450  
Alexandra, VA 22313-1450

RECEIVED  
FEB 11 2005  
CERTIFICATE OF CORRECTION

**REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT  
FOR PTO MISTAKE (37 C.F.R. § 1.322(a))**

1. Enclosed, in duplicate, is PTO/SB/44 (also Form PTO-1050), with at least one copy being suitable for printing.
2. Enclosed for your ease of reference is a copy of page 2 of the Amendment filed on August 2, 2002, where the error is shown correctly under Please Amend the Application to Read as Follows. The title of the application should read "System and Method for Controlling the Entry of Instructions into a Pipeline of an Instruction Processor". Applicant respectfully requests the error be corrected.
3. Enclosed for your ease of reference is a copy of page 33 of the Appellant's Brief filed on July 1, 2004, where the error is shown correctly in claim 11. In column 24, line 2 the terms "pipeline-including" should read "pipeline including". Applicant respectfully requests the errors be corrected.
4. Please send the Certificate to:

Name: Unisys Corporation  
Beth L. McMahon  
Address: P O Box 64942  
MS 4773  
St. Paul, MN 55164

Unisys Corporation  
(type or print name of assignee)

Beth L. McMahon  
Signature of person authorized to  
sign on behalf of assignee

- ☒ Assignment recorded on October 15, 1999

Reel 010322  
Frame 0862

Beth L. McMahon  
(type or print name of authorized person signing)

Attorney of Record  
Title of authorized person signing

- ☐ Recorded of assignment attached.

FEB 15 2005

- ☐ Recorded of assignment attached.  
☐ Attached is a "STATEMENT UNDER 37 CFR 3.73(b)," establishing the right of the assignee to take action in this case.

Respectfully submitted,

*Beth L. McMahon*

Beth L. McMahon  
Attorney for Applicant  
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BLM/eav

I hereby certify that this correspondence is being deposited in the United States Postal Service as first class mail in an envelope addressed to: Attn: Certificate of Correction Branch, Commissioner for Patents, Alexandria, VA 22313-1450 on February 2, 2005

\_\_\_\_\_  
Emily Vogt  
Legal Assistant

*Emily Vogt*  
\_\_\_\_\_  
Signature

\_\_\_\_\_  
February 2, 2005  
Date of Signature

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(Also Form PTO-1050)

## UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATION OF CORRECTION

PATENT NO : 6,839,833  
DATED : January 4, 2005  
INVENTOR(S) : Thomas D. Hartnett, John S. Kuslak and Leroy J. Longworth

It is certified that error appears in the above-identified patent and that said Letters Patent hereby corrected as shown below:

In the title:

The terms "Pipeline Depth Controller for an Instruction Processor" should read --System and Method for Controlling the Entry of Instructions into a Pipeline of an Instruction Processor--.

In the claims:

Claim number 11, Col. 24, line 2 : the terms "pipeline-including" should read --pipeline including --.

MAILING ADDRESS OF SENDER:  
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PATENT NO. 6,839,833

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PATENT NO. 6,839,833

PLEASE AMEND THE APPLICATION TO READ AS FOLLOWS:

Please change the title of the Application to "SYSTEM AND METHOD FOR CONTROLLING THE ENTRY OF INSTRUCTIONS INTO A PIPELINE OF AN INSTRUCTION PROCESSOR".

IN THE SPECIFICATION:

10 Please amend the Abstract of the Invention with this paragraph for the paragraph that appears on page 44.

15 A programmable pipeline depth controller is provided to control the number of instructions that begins execution within an instruction pipeline of an instruction processor within a predetermined period of time. The pipeline depth controller of the present invention includes a logic sequencer responsive to a programmable count value. Upon being enabled, the logic sequencer generates a pipeline control signal to selectively delay the entry of some instructions into the instruction pipeline so that the number of instructions that begins execution within the instruction pipeline during the predetermined period of time following the enabling of  
20 the logic sequencer is equal to the count value.

**Claim 11:**

1 11. For use in an instruction pipeline of an instruction processor, the instruction  
2 processor to execute instructions that are part of the instruction set of the instruction  
3 processor, the instruction pipeline being adapted to initiate the execution of a  
4 variable number of instructions, up to a predetermined maximum number of  
5 instructions, within a predetermined period of time when the instruction pipeline is  
6 operating in a default mode, and whereby up to said predetermined maximum  
7 number of instructions may be executing simultaneously within the instruction  
8 pipeline, the instruction pipeline including a pipeline controller to generate a pipeline  
9 control signal for temporarily preventing ones of the instructions from entering the  
10 instruction pipeline, a method of utilizing the pipeline controller to control the number  
11 of instructions for which execution is initiated by the instruction pipeline within the  
12 predetermined period of time, comprising the steps:  
13 providing a count to the pipeline controller; and  
14 utilizing the pipeline controller to selectively assert the pipeline control signal  
15 to cause the instruction pipeline to initiate the execution of the number of instructions  
16 specified by said count within a period of time equal to the predetermined period of  
17 time.

**Claim 12:**